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Interfacial delamination and fatigue life estimation of 3D solder bumps in flip-chip packages

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Abstract

Detailed three-dimensional finite element analysis was carried out for area-array solder-bumped flip-chip packages. The analysis enabled determinations of accurate three-dimensional effects on stress distributions as well as local fracture behaviors under thermal load. The 3D analysis also estimated thermal fatigue life of solder bumps. Since dimensions of various components span more than three orders of magnitude, the multi-scale finite element models were utilized to elucidate detailed deformation state near solder bumps. The global-local approach identified of critical solder bumps due to the overall deformation and investigated of interfacial delamination at microstructural level. The local model contained a single solder bump and sub-micron UBM layers. The two-step modeling approach enabled accurate fracture analysis otherwise difficult in large 3D models. Our analysis found the crack driving force and preferred delamination direction based on the 3D J-integral calculations. Shear deformations within and surrounding solder bump connectors were also investigated. The results revealed higher deformation in the 3D model than those predicted from 2D models. Additionally, the strain components were different. This has an important implication on the plastic flow characteristics during cyclic loading. Our model estimated about 25% greater steady-state shear strains in the 3D model than those in the 2D models. This result suggests a much shorter fatigue life than that based on the 2D analysis.
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1. Introduction

Due to high I/O density capability, small profiles, and good electrical performance, area-array solder-bumped flip-chip technology is increasingly used in the electronics industry [1]. Extensive research and development efforts have been devoted to provide reliable products with higher package density and performance. Failure analysis is one of the very difficult issues among them [2]. Typical failure modes observed in flip-chip packages include solder fatigue, interface delamination, and die cracking [3]. Our current research interests focus on the interfacial delamination and the fatigue behavior of solder-bumped flip-chip packages. While the underfill related fracture toughness has been studied in the past [2,4,5], local delamination, especially those at interfaces with solder bumps, is of more significance for understanding the circuit failure. Our previous work presented detailed 2D analysis on local fracture behaviors [6]. The current analysis extends this analysis to full 3D geometry and also includes detailed investigations on the fatigue life prediction.

Detailed modeling of sub-micron layers of under-bump metallurgy (UBM) is essential since the material mismatch causes stress concentrations and may lead to fracture initiation and propagation [7–10]. But the construction of finite element model detailed enough to resolve accurate stresses near delamination is difficult due to the complex geometrical design of the packages. In flip-chip packages, relevant component length scales range from sub-micron layers to tens of millimeter overall package dimensions. Thus, in order to achieve accurate determination of local stress and fracture behaviors that are influenced by property mismatches of

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global components (e.g., chip and substrate) as well as local components (e.g., solder bump and UBMs), two models at different scales are adopted for the current multi-scale finite element analysis (MS-FEA). The global-local approach is particularly essential for 3D analyses where computational requirements are more significant. Without the multi-scale modeling, it would not be possible to compute accurate fracture parameters near solder bumps since element sizes must be substantially small with respect to the components' dimensions. In the current study, first a global model for the entire flip-chip package containing many solder bumps is designed, and then a refined local model with single solder bump is constructed. The global model elucidates deformation caused by the mismatch of the die and substrate. In the cell model, the deformation surrounding a solder bump is transferred as the prescribed boundary conditions, which enables investigations of detailed stress state as well as the 3D interfacial delamination.

Past studies have investigated the thermal fatigue life of various packages. Although earlier 3D analyses exist, due to computational limitations, many models were not as refined as those typically used for 2D analyses [3,11–13]. It is important to quantify differences between 2D and 3D results and use them for the fatigue life estimations. The reliability and the fatigue life of flip-chip packages are directly affected by the magnitude of shear strain within solder bumps [14]. The modified Coffin–Mason law is commonly used approach to estimate the life [15–18]. Utilizing this method, the current investigation computes the steady-state shear deformation from the 3D global model to determine the number of thermal fatigue mean cycles. In the analysis, the maximum variation of strains as well as the average strain variation during steady-state cycles is used as the input. The both fracture analysis and fatigue life estimation should increase the understanding of possible failure mechanisms of flip-chip packages and clarify actual 3D effects.

2. 3D multi-scale computational procedure

2.1. Flip-chip geometry and global model

In the current investigation, a typical area-array solder-bumped flip-chip package is modeled to carry out the elastic–plastic global-local thermal–mechanical analysis. The model represents a test chip manufactured by Microfab Technology Pte. Ltd in Singapore and the material properties are discussed in Section 2.3. Although the details of flip-chip configurations vary models to models, the overall geometries are similar, and the results reported here should be useful for other configurations. The chip dimensions are 5 mm × 2.5 mm × 0.625 mm, and it is attached to the FR-4 substrate with 190 solder bumps. Between the die and substrate, the underfill FP2546 was used to reinforce the bonding. There is a 90 μm clearance between the chip and substrate. Each solder bump has the maximum diameter of 100 μm with 250 μm pitch. Using the geometrical symmetry, only one-quarter of the overall package is modeled as shown in Fig. 1. The substrate thickness influences the magnitudes of strains due to thermal mismatch. In general, the shear strains near the solder bumps increase as substrate thickens due to larger constraint [6]. Here it is chosen as 1.58 mm. The quarter model contains 45 full and 5 half solder bumps.

A considerable effort was required to mesh the complex model as shown in Fig. 2. First, elements near the chip–substrate interface are kept small to resolve high stresses. Second, an identical mesh is repeated in a small hexahedral box to enclose each solder bump. This process ensures the consistency condition of subsequent cell analysis where displacements from the global model are prescribed as boundary conditions. Within each box, there are about 600 eight-node elements. The entire mesh contains approximately 52,000 eight-node elements and 58,000 nodes. At the global scale, the UBM, Al bond pad, and the passivation layers were not included but were modeled in the cell mesh. To better illustrate the geometry, the top and cross-sectional views of the one-quarter package are shown in Fig. 3. Here *A–D* indicate the four corner solder bumps, which will be used to label solder positions in the following analyses.

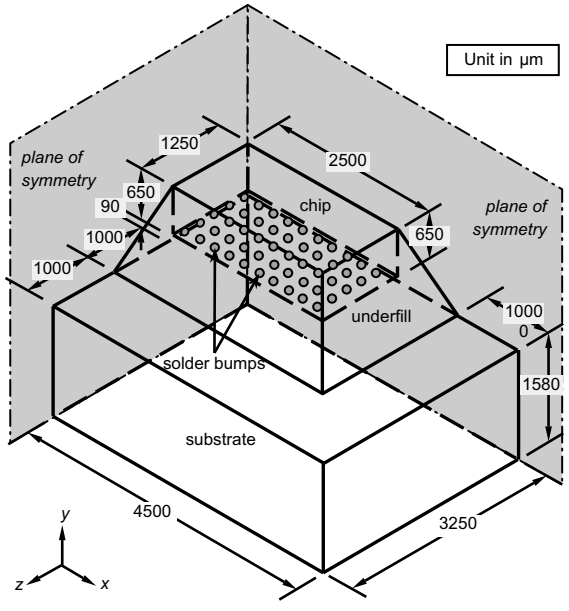

Fig. 1. One-quarter of 3D flip-chip package model used in the analysis. Dimensions and locations of various components are indicated.

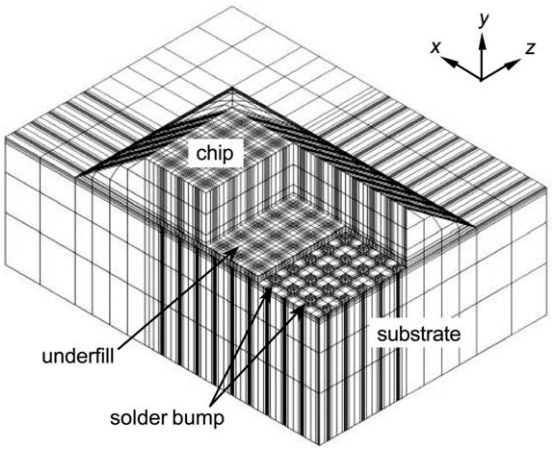

Fig. 2. Finite element mesh of the quarter model. Note elements are removed to show the interior mesh for solder bumps and underfill.

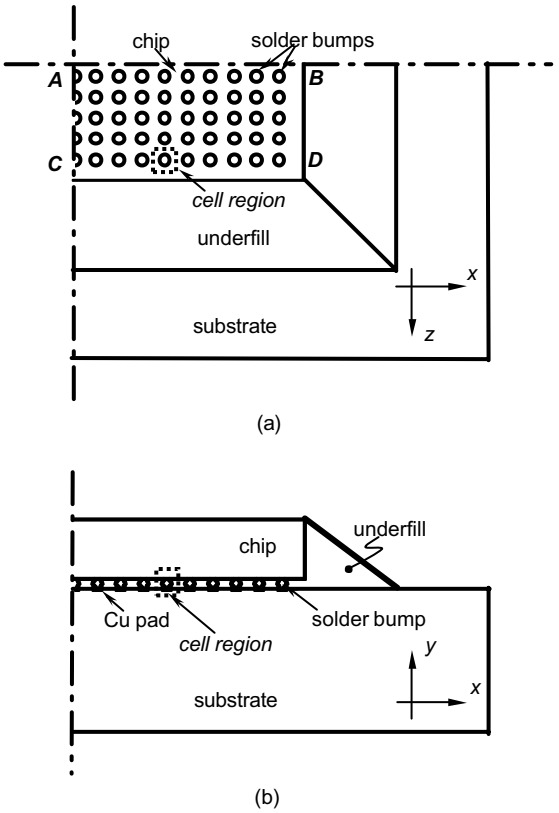

Fig. 3. (a) Top and (b) cross-sectional views of the flip-chip package. Cell region containing single solder bump is depicted. *A–D* indicate the corner solder bumps.

A 2D global model is also employed for the comparison study. It exactly models the cross-section of the 3D model as shown in Fig. 3(b). This minimizes any discrepancy arising from the mesh design. Detailed model please refer to [4].

2.2. Celllocal model

A more detailed 'cell model' is constructed for analyzing the local stress and interfacial fracture behaviors. As shown in Fig. 4, a single solder bump with two layers of UBM, Ni with 2.2 μm thickness and Cu with 7.3 μm thickness, are modeled here. An actual UBM contains additional layers (e.g., Au, Zn). These extremely thin layers (<0.1 μm) are not modeled here because of their limited mechanical influence [6]. On the chip side, the thickness of Al bond pad and Si_3N_4 passivation layer are 0.5 and 1.0 μm, respectively. In constructing the finite element mesh, elements representing the UBM and along interfaces are kept very small. Sufficiently small elements are required because of the possible stresses singularity and 3D fracture analysis. The size of the smallest elements is about 0.2 μm. The finite element mesh of the entire cell model is constructed with about 20,000 eight-node brick elements, 70,000 four-node tetrahedron elements, and approximately 35,000 nodes. The tetrahedron elements were necessary to generate the mesh in the complex regions. Although only one-half of

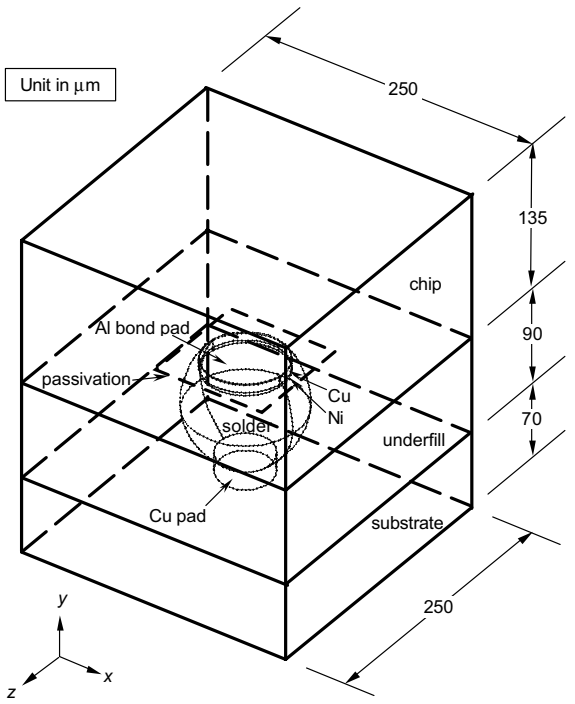

Fig. 4. Cell model containing single solder bump for detailed stress and fracture analysis. Dimensions and locations of various components are indicated.

the cell model is shown for clarity in Fig. 5, the full geometry was used for the analysis. This cell model may represent any solder bumps in the package with appropriate displacement boundary conditions prescribed on its external surfaces.

2.3. Material properties

The materials considered here are commonly used in various electronic packages [19,20]. At high temperature, some of them are sensitive to temperature. However we assumed their properties to be independent of temperature and loading rate since these factors not only make the analysis more complex but also introduce an additional parameter. As shown in Table 1, the eutectic solder (63Sn/37Pb) is the only material treated as elastic–plastic since its yield stress ($\sigma_0 = 20$ MPa) is far below those of other materials. The linear plastic hardening slope at 1.0 GPa is assumed for the solder. All the other components are considered to be linear elastic materials. In the table, E is the Young's modulus, v is the Poisson's ratio, and CTE is the coefficient of thermal expansion.

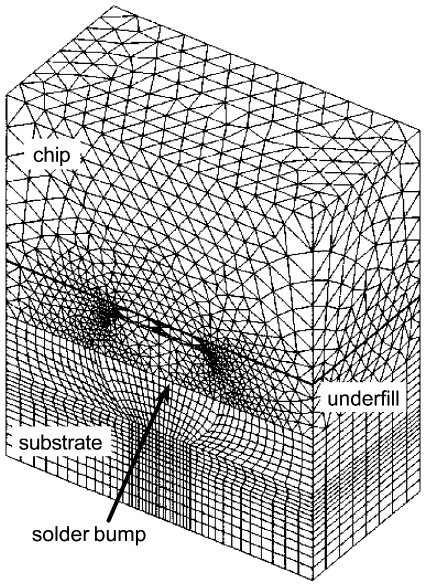

Fig. 5. Finite element mesh for the cell analysis. Only one-half is shown for interior element arrangements.

2.4. Loading conditions for global model

In the present analysis, initially a single temperature drop is imposed although flip-chip packages are subjected to several temperature variations during fabrication. To account for *stress relaxation* due to visco-plastic effects of actual solder, the initial temperature is set at 155 °C that is slightly lower than the eutectic temperature of solder (183 °C). At this temperature, no residual stresses are assumed to exist within the package (i.e., stress-free temperature). In the simulation, this temperature is gradually reduced to the room temperature at 20 °C, which causes thermal stresses to develop. Throughout the temperature drop, no transient heat transfer is considered and the temperature within the model is assumed to be uniform. About 20 time increments are taken to lower the temperature to ensure the accuracy. The temperature change is applied to both the global and cell models. In the global model, horizontal displacements normal to the symmetrical surfaces are set to remain 0 while no constraint is imposed on the bottom of substrate.

2.5. Loading conditions for cell model

The computed displacement field of the global model at the room temperature is interpolated and transferred to the cell model as its boundary condition as shown in Fig. 6. Both models were constructed in such a way to share the same physical surfaces but not the same nodal coordinates since many more nodes exist in the cell model. In order to find the magnitudes of displacement components $\boldsymbol{u}^{C}$ of a cell model's node, the displacements

Table 1
Material properties of components modeled in the package analysis

Materials	CTE (ppm/°C)	E (GPa)	v	σ_0 (MPa)
Chip (Si)	2.8	131	0.30	
Passivation (Si_3N_4)	2.9	325	0.24	
Bond pad (Al)	23.2	70	0.24	
UBM layer 1 (Cu)	16	117	0.30	
UBM layer 2 (Ni)	12.7	200	0.31	
Solder bump (63Sn/37Pb)	21	30	0.35	20
Underfill (FP2546)	33	8.5	0.28	
Substrate (FR4)	18	22	0.28	

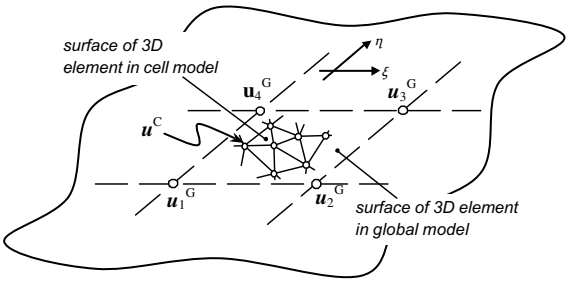

Fig. 6. Schematic of interpolation used to prescribed displacement boundary conditions for the cell model. At every node on the external surfaces of the cell model, displacement components $\boldsymbol{u}^{C}$ are interpolated from computed displacements $\boldsymbol{u}_1^{G}$–$\boldsymbol{u}_4^{G}$ of the global model.

of global model's nodes $\boldsymbol{u}_\alpha^{G}$ are interpolated with the bilinear interpolation functions as,

$$\boldsymbol{u}^{C} = \sum_{\alpha=1}^{4} N_\alpha(\xi,\eta)\boldsymbol{u}_\alpha^{G} \tag{1}$$

Here N_α are the interpolated functions, ξ and η are the local in-plane coordinates on the surface. The interpolation is carried out for every cell model's node on the six separate external sides of the volume. As in the global analysis, the magnitudes of the imposed nodal displacements are gradually increased while the temperature is gradually reduced ($\Delta T = -135$ °C) simultaneously over 20 increments.

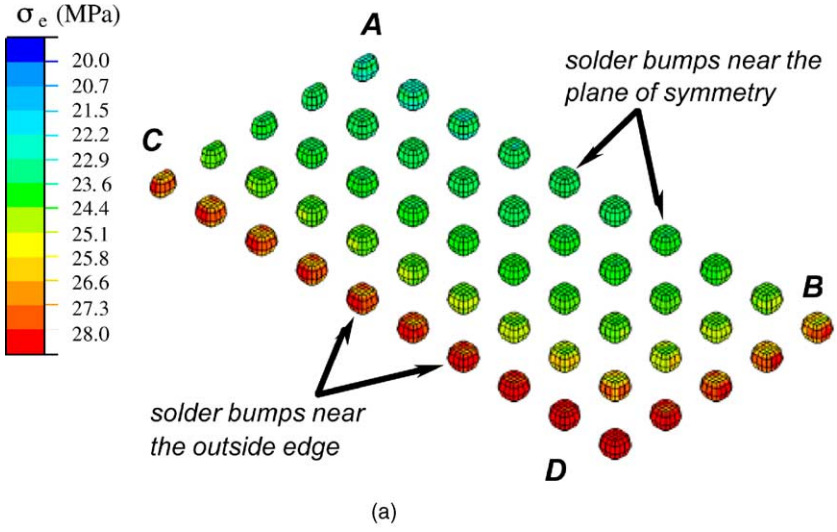

Fig. 7. (a) Shades of effective stress, and (b) shades of equivalent strain in solder bumps after $\Delta T = -135$ °C.

3. Stress and deformation at global level

3.1. Average strains in solder bumps

First, a single temperature drop condition was considered with the global model. Fig. 7 shows the distribution of effective stress and equivalent plastic strain, respectively, among the solder bumps after the temperature drop of 135 °C. The other package components (e.g., underfill) were removed to illustrate the individual bumps clearly. Here, '*AB*' indicates the row of solder bumps close to the plane of symmetry, while '*CD*' is the row near the package edge (see also Fig. 3). They show the variations of stress and strain states in the different bumps. The maximum stress and strain are found in the corner bump *D* while the lowest occurs at the center bump *A*. In between, they vary gradually as shown by changes in the colors (from *C* to *D* and from *B* to *D*). The effective stress is about 20% higher in the bump *D* than in the bump *A*. The difference is much greater in terms of plastic strain. The corner bump *D* experiences well above 1% strain, which is three times greater strain than that of the center bump *A*. This large strain has a significant implication on its failure and fatigue characteristics.

To better quantify the variations of deformation among solder bumps, average shear strains within each solder bump were computed. Since the shearing is the major contribution in the solder bump failure, it directly controls the package reliability. The average shear strains within a solder bump can be obtained by either taking the volume average of elements or integrating the nodal displacements over the boundary surfaces of the solder bumps via the divergence theory as,

$$\gamma_{ij}^{\text{ave}} = \frac{1}{V}\int_V \gamma_{ij}\,\mathrm{d}V = \frac{1}{V}\int_S (u_i n_j + u_j n_i)\,\mathrm{d}S \tag{2}$$

Here γ_{ij} are the strain components of all the elements within the solder bump region and V is the bump volume. Also, u_i and n_j represent nodal displacements and the normal direction perpendicular to the bump surface S. A similar procedure was used to calculate the average strains in 2D models. The averages shear strains within the solder bumps along two rows are shown in Fig. 8. The strains of solder bumps along the symmetry row (*A–B*) and the edge row (*C–D*) are shown as the functions of distance away from the center plane, respectively. Note the directions of coordinates shown in Fig. 7(b). Each symbol represents the mid-point location of a solder bump. Along both rows, the out-of-plane shear γ_{xy} increases significantly from the center to the edge (with y being the out-of-plane direction). Meanwhile the in-plane shear γ_{xz} remains almost negligible everywhere. The behavior of the other out-of-plane shear γ_{yz} is interesting. It is very small along the symmetry row

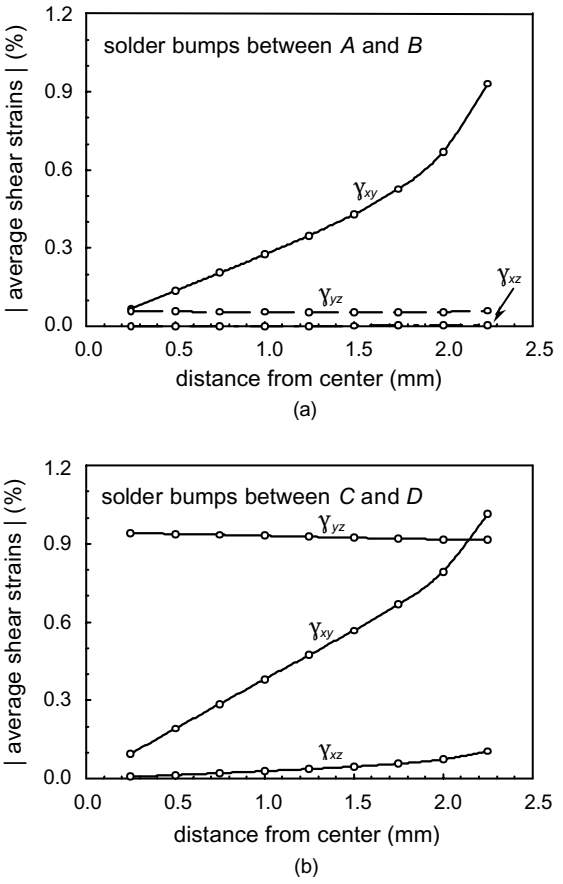

Fig. 8. Average shear strain components within solder bumps after $\Delta T = -135$ °C are shown as functions of distance away from the mid-point: (a) along the symmetry plane (between *A* and *B*) and (b) along the outside edge (between *C* and *D*).

(*A–B*) but consistently large along the near edge row of solder bumps (*C–D*). This is clearly the 3D effect as the shearing along the z direction causes the strain, which would not appear in the 2D models. Indeed this shear component increases from *A* to *C* (or *B* to *D*) although not shown here. Even though the shearing on the other plane was expected, its high magnitude is rather surprising. At the corner solder bump (at 2.25 mm from the center in Fig. 8(b)), the y–z component of shear (γ_{yz}) is nearly as high as the other component (γ_{xy}) despite the chip length along the z direction is only half as long as along the x direction.

3.2. Comparison with 2D models

In order to quantify the effects of 3D geometry, the average equivalent shear strains of solder bumps were compared with those of the 2D models. It uses the cross-sectional model shown in Fig. 3(b). The equivalent shear

strain represents the effective shear deformation caused by all strain components including the normal components. It is the primary parameter used in the fatigue analysis. The equivalent shear strain is given by,

$$\gamma_{eq} = \sqrt{\tfrac{2}{3}}\Big[(\varepsilon_x - \varepsilon_y)^2 + (\varepsilon_y - \varepsilon_z)^2 + (\varepsilon_z - \varepsilon_x)^2 + \tfrac{3}{2}(\gamma_{xy}^2 + \gamma_{xz}^2 + \gamma_{zx}^2)\Big]^{1/2} \quad (3)$$

The above strain was computed at every element within a solder bump and the average value of each bump was determined thereafter. The results along the near edge (*C–D*) row and the near symmetry (*A–B*) row are shown in Fig. 9(a). As expected, the magnitudes are significantly higher for the solder bumps along *C–D* due to the large γ_{yz}. In the same plot, corresponding 2D results under plane strain and plane stress conditions are also shown. Here, two key observations can be made. First, γ_{eq}^{ave} of 3D model along *A–B* lie between γ_{eq}^{ave} of the plane strain and plane stress models. This is consistent with many models where 3D results along symmetry planes fall between the plane strain and plane stress results. Second, as the distance from the center is increased, the plane strain γ_{eq}^{ave} increases rapidly to reach close to γ_{eq}^{ave} of 3D model (*C–D*) at the corner. At first sight, it is inconsistent since γ_{yz} is large in the 3D model (Fig. 8(b)) while $\gamma_{yz} = 0$ in the plane strain. However, after inspection of individual strain components, it was found that the constraint of $\varepsilon_z = 0$ in the plane strain case causes large equivalent shear strain in (3). It is important to note that magnitudes of individual strain components of 3D model and the plane strain model are *quite different* even though γ_{eq}^{ave} are similar. In the 3D model, two shear strain components are large while all three normal strain components are similar. In the plane strain model, one shear strain component is large and there are two large normal strains and one zero normal strain component. Collectively, both yield about the same γ_{eq}^{ave}. But these different strain states generate different plastic flows during cyclic loading and as a consequence, different estimated fatigue life. This will be discussed in Section 5.

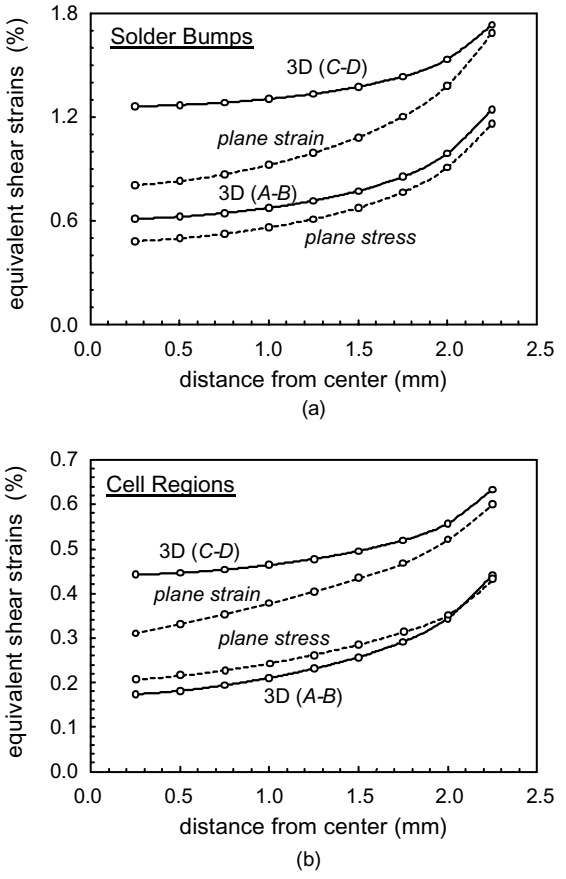

Fig. 9. Comparison of average equivalent shear strains along row *C–D* and *A–B*. Plane strain and plane stress solutions are also shown for comparison: (a) within solder bumps and (b) within cell regions.

In order to quantify the amount of shear deformation within a region which includes components other than the solder, the average equivalent shear strain of cell region defined earlier was also obtained. In addition to a single solder bump, the cell region contains the copper pad, parts of chip, substrate, and underfill. The results are shown in Fig. 9(b). Similar behaviors of γ_{eq}^{ave} as those for the solder bumps are observed, but with about half of the magnitudes. Although the solder bump is surrounded by the stiffer components, the strain field is not uniform in the region. In fact, there is an intense shearing along the mid-height of the solder bump, which the strain in the solder bump to be significantly higher than that for the whole cell region. Essentially, γ_{eq}^{ave} of the cell regions represent the effective shearing due to the mismatch in the CTE of the chip and the substrate. In fact, the shear strains approximated from simple elastic models agree well with those reported here. However, the comparison of the two plots in Fig. 9 suggests that actual shear deformation within the solder bump is much higher than those predicted from the elastic models. Investigation of stress state near the solder bump requires more detailed mesh and the following local/cell analysis reveals the stress concentration and the failure mechanisms.

4. Local stress and delamination analysis

4.1. Stress state near solder bump and UBM

As described in Section 2.5, the computed displacements in the global analysis were transfer to the cell model as the boundary condition. To verify the consistency

of the global–local modeling, the total internal strain energies of the two models were computed within the cell region of the corner bump. With the temperature drop of $\Delta T = -135$ °C, the energies are 2.72×10^{-6} J for the cell of global model and 2.74×10^{-6} J for the local model with the difference being less than 1%. This should be an acceptable consistency between the two models. The global–local procedure can be applied to any solder bump in the model without remodeling the finite element mesh. Since the corner bump (D) experiences the largest shear, this bump was chosen for the local analysis. First, the analysis was carried out without a delamination or flaw. Then, the fracture analysis was carried out with an embedded flaw. The computed effective stress in Fig. 10 shows the internal stress on the cross-sections of components. The cross-sectional faces lie on the x–y plane. The chip, substrate and underfill are not shown for clarity. Although the solder bump is highly strained, the yielding (at $\sigma_0 = 20$ MPa) keeps its stresses to be low. On the other hand, very high stresses are observed in the UBM, the Al bond pad and the passivation layer. In addition, the interfaces of solder bump and Cu pad show high stresses and can be potential failure sites. It is worth noting that these stresses are not rotationally symmetrical. The stresses are higher along certain directions and likely to influence directions of failure growths.

Although not shown here, other stress and strain components were inspected to determine the stress and

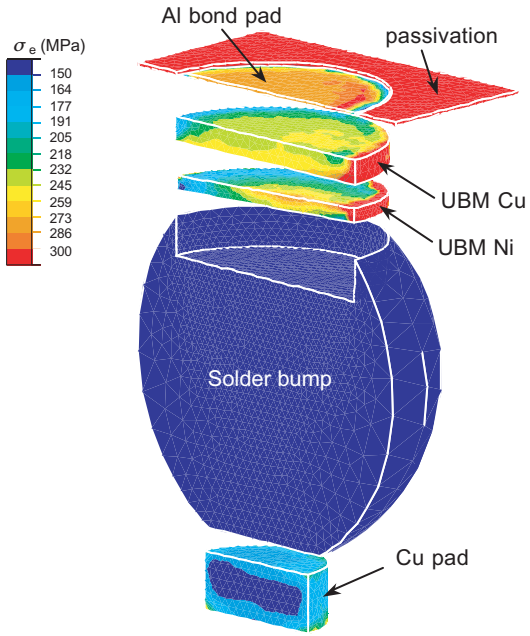

Fig. 10. Shades of internal effective stress near the solder bump including UBMs after $\Delta T = -135$ °C. The cross-sectional image is shown for better view.

deformation state surrounding the solder bump. The present modeling procedure easily allows similar analyses to be repeated for identifications of critical sites at other solder bump regions as long as proper boundary conditions are prescribed.

4.2. Interfacial delamination

In many packages, failure due to loss of electrical connection occurs at or near the interfaces with the solder bump. Generally, bonding between different materials is weak and its fracture resistance is lower than those of bulk materials. In the current analysis, a 3D interface crack is assumed to exist between the solder bump and the copper pad. Although this interface was chosen arbitrary, the current computational allows modeling of cracks at other interfaces (e.g., between UBM and Al pad). Here, it is assumed that the embedded crack shape to be half-penny shaped as shown in Fig. 11. This shape represents the *mid-way* flaw configuration to the total electrical connection failure. As shown by the directional dependence of stress distribution in Fig. 10, it is expected that the fracture parameters along the crack front vary according to the crack direction. In order to investigate such an effect, the fracture analysis is carried out for various normal directions of crack front indicated by θ in Fig. 11(b).

For each crack model, two fracture parameters are computed along the 3D crack front. They are J-integral and the phase angle. Since the interfacial delamination is between the elastic–plastic solder bump and elastic Cu pad, the elastic stress intensity factors are not applicable. Using the computed displacement and stress fields [21,22], J at each node along the crack front is obtained as

$$J = \frac{\int_V \left(\sigma_{ij}\dfrac{\partial u_i}{\partial x_k}\dfrac{\partial q_k}{\partial x_j} - W\dfrac{\partial q_k}{\partial x_k}\right)\mathrm{d}V}{\int_{\delta s} q_k(s)\mu_k(s)\,\mathrm{d}s} \tag{4}$$

Here σ_{ij} and u_k are the Cartesian components of the stress and displacement, respectively, V is an arbitrary volume which enclosed the crack segment, s is the location of the crack front, and $q_k(s)$ is a weighting function of position. Also, $\mu_k(s)$ represents a unit vector perpendicular to the crack front over the segment δs, and W is the strain energy density defined as the mechanical work of strain excluding the energy due to thermal strain. For any interfacial cracks, it is important to determine the *mode-mixity* since it influences the toughness of the interface [23]. In general, it is represented by the phase angles ψ and ϕ. For elastic–plastic models, they are computed from the ratio of the shear to normal traction ahead of the crack tip (i.e., mode II or III over mode I). In the current analysis, the phase

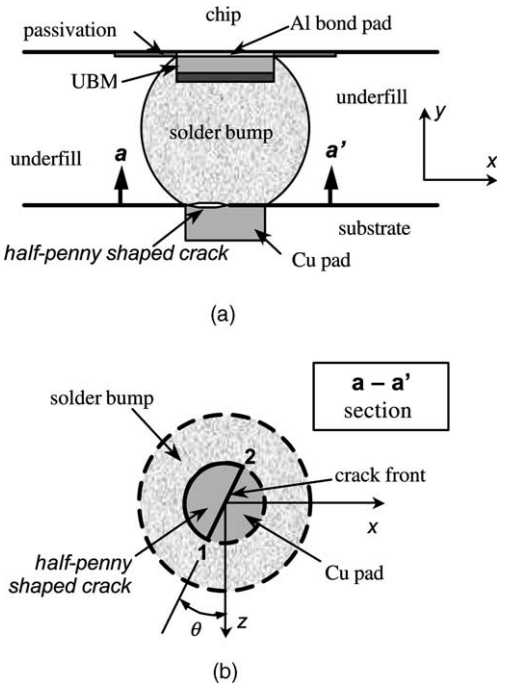

Fig. 11. Delamination between the solder bump and the Cu pad is modeled as a half-penny shaped crack. Relative location is shown in (a) side view, and (b) top-view through a–a' section. The orientation of crack front relative to the z-axis is shown by the angle θ.

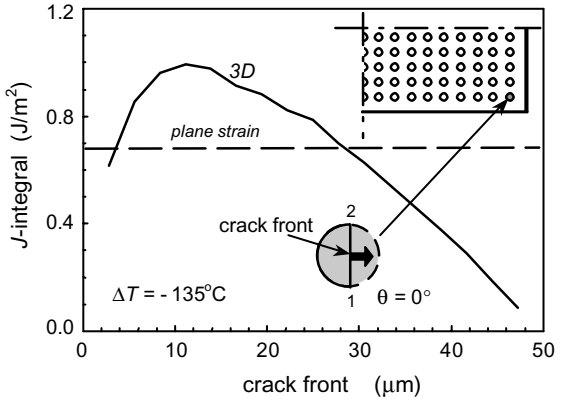

Fig. 12. Variation of J-integral along 3D interfacial crack front between solder bump and copper pad is shown for the $\theta = 0°$ orientation (measured from 1 to 2). The solder bump location at the corner is illustrated. The peak J is about 40% higher than the value estimated from 2D plane strain analysis.

angles can be determined from the stresses ahead of the crack as [24],

$$\psi \approx \tan^{-1}\left(\frac{\sigma_{12}}{\sigma_{22}}\right) \quad \text{and}$$
$$\phi \approx \cos^{-1}\left|\frac{\sigma_{23}}{\sqrt{\sigma_{22}^2+\sigma_{12}^2+\sigma_{23}^2}}\right| \tag{5}$$

Here '1' represents the crack direction, '2' is normal to the crack face, and '3' is perpendicular to the 1–2 plane. Generally, the characteristic length scale must be defined when reporting the phase angles. In the current analysis, it is set as $L = 2$ μm which is one element ahead of the crack front.

At first, the crack orientation of $\theta = 0°$, is considered and the J-integral was calculated over 25 nodes along the crack front as shown in Fig. 12. In the same figure, the corresponding value from the plane strain model is indicated. Although the average J from the 3D model is similar to this value, the peak value about 40% higher. This suggests a greater possibility of failure propagation from on the 3D analysis. The actual failure event depends on the toughness of solder–copper interface. It is expected that the peak value of $J \cong 1$ J/m^2 is close to the actual toughness of such an interface. The computed phase angles are $\psi = 30$–$35°$ and $\phi = 65$–$70°$ along the entire crack front while for the plane strain model, it is $\psi = 55°$ (and $\phi = 0°$). Generally, the toughness is lower with smaller phase angle, and hence, the results suggest a greater likeliness of crack propagation based on the 3D results.

The directional dependence of the fracture parameters was investigated with different crack orientation angle θ. In Fig. 13(a), the results from $\theta = 0°$, 45°, and 90° are shown. These cracks propagate from the center of the package to the edges or in the *outward* direction. It is interesting to observe the variations of J along the crack front are not consistent and the peaks occur at different crack front positions. It appears the peak occurs near the exterior of the chip. For the 0° crack, it is close to the end '1' which is nearer to the edge of chip, and for the 90° crack, it is close to the end '2' which is nearer to the other edge. The cases of *inward* delamination directions are shown in Fig. 13(b). Here, $\theta = 180°$, 225°, and 270° are chosen. In contrast to the outward cracks, their variations are very similar. All of them have the peak J occurring at the mid-point of the crack front. The value $J \cong 1.1$ J/m^2 is also somewhat higher than those observed for the *outward* cracks. These results show similar peak J values regardless of the crack front direction. In addition, the peak J in the any configurations is substantially larger than the one predicted from the plane strain analysis. Although the current fracture analysis revealed important 3D features of embedded delamination, precise prediction of crack propagation behavior is difficult since it may depend on many factors including the shape of crack front.

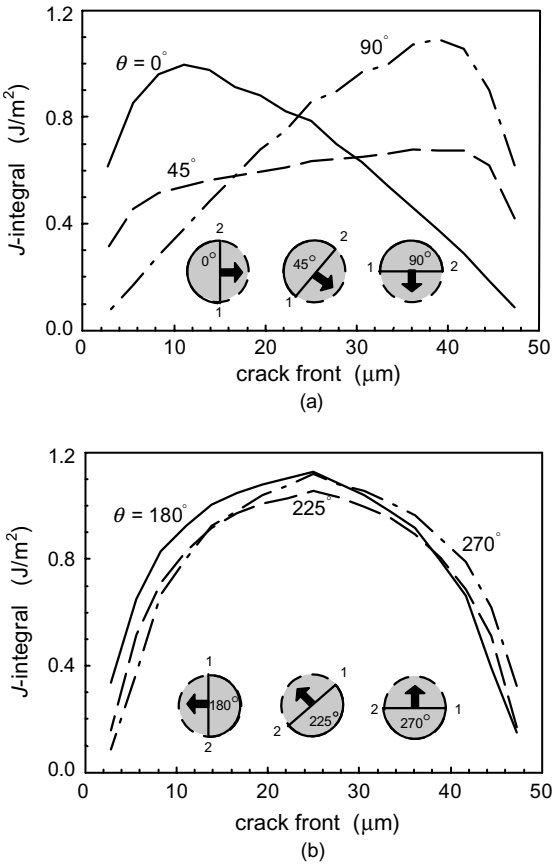

Fig. 13. Variations of J are shown for six different crack front orientations: (a) $\theta = 0°$, 45°, 90° and (b) $\theta = 180°$, 225°, 270°. All of them are for the solder bump at corner under $\Delta T = -135$ °C. The locations of peak J vary for different orientations.

5. Thermal cycle analysis

The reliability of flip-chip packages is often dictated by the thermal fatigue life of solder bumps. The solder fatigues due to much higher deformation cycles than other components. According to our 2D calculation, the average equivalent shear strains of various components in the corner bump region are: chip 0.12%, Cu pad 0.33%, substrate 0.47%, underfill 1.3%, and solder 1.68%. Thus the shearing is much higher in the solder bump. The most commonly used strain-life approach to estimate the fatigue life is the Coffin–Mason law [25]. This model is utilized in the present analysis to predict thermal fatigue lives of solder bumps based on isotropic and linear kinematic hardening plastic assumption.

5.1. Coffin–Manson rule

The Coffin–Manson rule is a linear relationship between the logarithm of the plastic strain amplitude, $\Delta\varepsilon_p$, and the logarithm of the number of load reversals to failure [25]. Engelmaier [15] proposed a modified version of the rule for near eutectic Sn–Pb solders subjected to primary shear loading as

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma_{eq}}{2\varepsilon_f}\right)^{(1/c)} \tag{6}$$

Here, N_f is the mean cycle to failure, $\Delta\gamma_{eq}$ is the variation of equivalent shear strain during cycle, ε_f is the fatigue ductility coefficient which is generally taken as $\varepsilon_f = 0.325$, and c is the fatigue ductility exponent which is approximately -0.5 [18,26]. In the current analysis, Engelmaier's empirical expression, $c = -0.442 - 6 \times 10^{-4} T_{mean} + 1.74 \times 10^{-2} \ln(1+f)$ is adopted. In the equation, T_{mean} is the mean cyclic temperature (i.e., $T_{mean} = (T_{max} + T_{min})/2$), and f is the cyclic frequency ($1 < f < 1000$ cycles per day). Here the temperature range is between 20 and 125 °C and the cyclic frequency is assumed as $f = 1$, and $c = -0.473$ can be obtained.

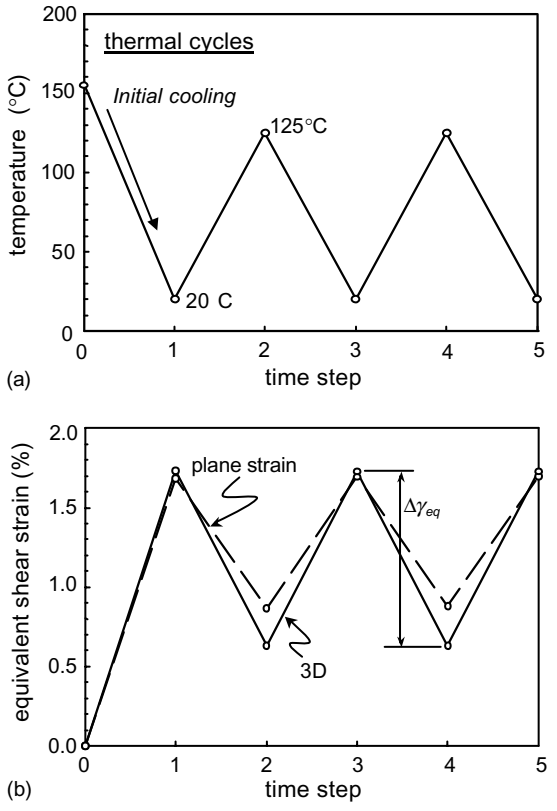

Fig. 14. (a) Thermal cycles imposed to flip-chip package. (b) Average equivalent shear strain in the solder for 3D and plane strain models during the cycle. The amplitude $\Delta\gamma_{eq}$ for 3D model is noted.

5.2. Fatigue life estimation

Often, the strain changes in the Coffin–Mason rule are obtained from single temperature drop calculations. Although it should provide with an estimate, better estimates can be obtained from multiple thermal cycles calculations since the solder undergoes complex plastic deformation. Here, as described in Section 3, the initial stress-free temperature is set at 155 °C. Then it is lowered to the room temperature 20 °C. The subsequent heating raises the temperature to 125 °C [17]. Afterward it is again lowered to 20 °C. These temperature cycles are illustrated in Fig. 14(a). The cycles between 20 and 125 °C is repeated until the change in the equivalent shear strain reaches a steady-state value. The cyclic analysis was conducted with the global model. At the end of each temperature reversal, the equivalent shear strains of all elements within the solder are computed. Initially, the plastic hardening law for the solder was assumed to be isotropic. However since some report that the solder exhibits kinematic hardening condition [27], we have also modeled the kinematic hardening law for the solder.

For isotropic-hardening solder model, the average results of γ_{eq} of the corner solder bump (D) are shown in Fig. 14(b). It is noted that the 1st step result is identical to the one shown in Fig. 9(a). The difference between two steps is recorded as the change of γ_{eq}^{ave} between load reversals. It appears that $\Delta\gamma_{eq}^{ave}$ converged to about 1.1% in a few steps and this was taken as the steady-state value. In the same figure, the corresponding plane strain results are included. It is interesting to observe that although the initial rise in the γ_{eq}^{ave} is very close to that of the 3D model, subsequent change in γ_{eq}^{ave} is significantly smaller. The difference in $\Delta\gamma_{eq}^{ave}$ between the 3D and the plane strain models can be explained by the different individual strain component as discussed in Section 2. Suppose the simulation of *cyclic* loading were not carried out but only a *single temperature drop* ($\Delta T = 105$ °C) was calculated. It would predict $\Delta\gamma_{eq}^{ave} = 1.3\%$, which has about 20% error. Thus it is important to perform the cyclic thermal loading to obtain the steady-state value. The complete calculation results of $\Delta\gamma_{eq}^{ave}$ and γ_{eq}^{max} at each thermal cycle are tabulated in Table 2. The latter parameter corresponds to the maximum $\Delta\gamma_{eq}$ observed in the solder. Although difficult to be obtained, it actually represents the fatigue life of the solder connection. The mean cycles to failure were estimated from the modified Coffin–Mason rule (6) using the steady-state $\Delta\gamma_{eq}$. The estimation gives N_f to be 2020 cycles for the 3D model. The results from the plane strain model are

Table 2
Amplitudes of equivalent shear strain change in the corner solder bump during thermal cycles with the isotropic-hardening model

Load steps	Temperature change (°C)	3D model		Plane strain model	
		Average $\Delta\gamma_{eq}$ (%)	Maximum $\Delta\gamma_{eq}$ (%)	Average $\Delta\gamma_{eq}$ (%)	Maximum $\Delta\gamma_{eq}$ (%)
1	155 → 20	1.731	2.023	1.683	1.943
2	20 → 125	1.104	1.267	0.818	1.012
3	125 → 20	1.101	1.272	0.830	0.977
4	20 → 125	1.100	1.270	0.818	0.965
5	125 → 20	1.100	1.270	0.822	0.969
Fatigue life N_f		2728	2020	5058	3486

The average value is from the entire solder while the maximum value corresponds to the largest strain change occurred within the solder bump. Estimated fatigue life is based on the steady-state value.

Table 3
Amplitudes of equivalent shear strain change in the corner solder bump during thermal cycles with the kinematic hardening model

Load steps	Temperature change (°C)	3D model		Plane strain model	
		Average $\Delta\gamma_{eq}$ (%)	Maximum $\Delta\gamma_{eq}$ (%)	Average $\Delta\gamma_{eq}$ (%)	Maximum $\Delta\gamma_{eq}$ (%)
1	155 → 20	1.731	2.018	1.684	1.865
2	20 → 125	1.193	1.385	0.994	1.133
3	125 → 20	1.194	1.379	1.00	1.108
4	20 → 125	1.194	1.383	0.998	1.111
5	125 → 20	1.194	1.380	0.998	1.105
Fatigue life N_f		2301	1691	3356	2663

The average value is from the entire solder while the maximum value corresponds to the largest strain change occurred within the solder bump. Estimated fatigue life is based on the steady-state value.

also listed. Since its $\Delta\gamma_{eq}$ is about 25% lower than the 3D value, the estimated fatigue life is 3486 cycles, which is 70% greater than the 3D model. These results suggest the considerable overestimation of thermal fatigue life by plane strain analyses as well as the importance of 3D models to obtain accurate variations of strains.

For the kinematic hardening solder model, the results of $\Delta\gamma_{eq}^{ave}$ and $\Delta\gamma_{eq}^{max}$ as well as corresponding estimated thermal fatigue lives are listed in Table 3. The estimation from maximum $\Delta\gamma_{eq}$ gives N_f to be 1691 cycles for the 3D model. The results from the plane strain model are about 20% lower than the 3D value and the estimated fatigue life is 2663 cycles, which is 60% greater than the 3D model. Due to higher strains, the fatigue life estimations with the kinematic hardening model are significantly less than those determined from the isotropic-hardening model.

6. Discussions

The current work presented a detailed procedure to carry out 3D delamination analysis and quantify the 3D effects of flip-chip packages. The fracture analysis utilized the multi-scale finite element approach, which is essential in large-scale three-dimensional fracture analysis. With detailed modeling of local/cell region, elements are small enough to determine accurate fracture parameters of 3D interfacial crack front. This approach is ideally suited for the flip-chip packages that contain many identically repeated solder bumps, and where large scale-difference exists.

The computed J-integral for the embedded interfacial crack between the solder bump and copper pad revealed important 3D characteristics. First, the peak J was higher than the corresponding value in the 2D model. Second, the variation of J is strongly dependent on the direction of crack. The latter fact may be used to predict preferred delamination phenomenon in actual package. The phase angles are also significantly larger than those estimated from the 2D model. In fact there is a very large mode III component in these cracks. Using similar approaches, one can optimize geometry and/or materials to resist delamination although accurate prediction of failure near the solder bumps and UBM requires the experimental determination of interfacial toughness.

The study also found significant 3D effects from the comparison study with the 2D solutions. First, the deformation magnitudes in the solder bumps were higher in the 3D model due to the existence of additional (out-of-plane) shear. More importantly, the deformation mechanisms differed substantially from those of the 2D model. Although both 3D and plane strain showed similar γ_{eq} under monotonic loading (at the corner solder bump), subsequent heating and cooling cycles produced difference $\Delta\gamma_{eq}$. Specifically, the relative magnitudes of individual strain components were not similar in the 3D and plane strain models, and it caused different plastic flow characteristics. In the 3D model, two large shear strain components controlled the plastic deformation, while a single shear strain and two normal strain components produced the plastic flow in the plane strain model. The former mechanism resulted 20% higher strain than the one predicted from the 2D model. This has a significant implication in the package reliability since the larger strain means the estimated fatigue life of the solder bump to be *only* 69% of the corresponding plane strain prediction. The present analysis also studied the different plastic hardening laws. The results of kinematic hardening model showed larger strains than those found with the isotropic-hardening model. This led to the lowering of the fatigue life estimation by about 15%.

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